What is claimed is:

Patent Claims

1. Method for masking first recesses (1) in a structure (4) having webs (4) with a high aspect ratio, comprising a set of recesses (1, 2) having different aspect ratios, in particular a semiconductor structure, having the following steps:
- a filling layer (5) is applied to the structure (1, 2, 4),
with the filling layer (5) being applied over a fixed distance beyond the webs (4) in such a way that a cavity (6) is formed in first recesses (1) having a high aspect ratio,
- the filling layer (5) is removed by means of a planar removal process into the area of the cavity (6) with the filling layer (5) being removed to a defined distance above the surface of the webs (4),
- the filling layer (5) is removed in an etching process, with the etching process also attacking in the cavity (6) and, owing to the cavity (6), the filling layer (5) being removed more quickly from the first recess (1) than from recesses (2) without a cavity (6), and with the etching process being stopped after removal of the filling layer (5) from the first recess (1), with the defined distance being chosen such that the webs (4) are not underetched in the area of a recess (2) with a low aspect ratio during the etching process.

2. Method according to Claim 1, characterized in that an isotropic etching method is used as the etching method.

3. Method according to one of Claims 1 or 2, characterized in that the structure (1, 2, 4) has webs (4), and in that a sacrificial layer (12) is applied to

the surface of the webs (4), before the application of the filling layer (5).

4. Method according to one of Claims 1 to 3, characterized in that a chemical/mechanical polishing method is used as the planar removal process.

5. Method according to Claim 4, characterized in that the defined distance is chosen to be greater than twice the maximum thickness (β) of the filling material (5) between a cavity (6) and the structure (4, 3).

6. Method according to one of Claims 1 to 5, characterized in that the structure (1, 2, 4) is formed from a silicon wafer (3).

7. Method according to one of Claims 1 to 6, characterized in that silicon oxide is deposited as the filling layer (5), using a TEOS process.

8. Method according to one of Claims 1 to 7, characterized in that silicon oxide is deposited as the sacrificial layer (12).

9. Method according to one of Claims 1 to 8, characterized in that the filling layer (5) is applied over a recess (2) with a low aspect ratio to above the height of the cavity (6).